Deliverable Number: D 21.06

Deliverable Title: Report on STFC and Jülich detector electronics hardware

Delivery date:	[36]
Leading beneficiary:	4
Dissemination level:	PU
Status:	Finished
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Project number:	283883
Project acronym:	NMI3-II
Project title:	Neutron Scattering and Muon Spectroscopy Integrated Initiative
Starting date:	1st of February 2012
Duration:	36 months
Call identifier:	FP7-Infrastructures-2011-1
Funding scheme:	Combination of CP & CSA – Integrating Activities

Description:

The ISIS and Jülich detectors developed in this JRA use 16-channel and 64-channel multi anode photomultiplier tubes (MA PMTs) respectively, to capture the scintillation light and convert it to electronic signals. In the ISIS systems the positions of neutron events are determined using a pattern recognition system. In the Jülich detectors the positions of neutron events are determined by a centre of gravity method in a PC. The differences in detector operation require different electronics solutions.

The ISIS detector electronics hardware

In the ISIS detectors the electronics consists of three types of components; 8-channel pre amp/comparator cards, an FPGA card that does the signal processing and a low voltage power supply card. The outputs signals from each of the pixels of the PMTs are fed into two 8-channel pre amp/comparator cards located at the back of the PMTs. Outputs from the comparators are fed to an FPGA card in the detector housing. In the original version of the electronics the FPGA selected for this card was a Cyclone 3 EP3C120 from Altera. In the FPGA, the digital signals are integrated and shaped and then interrogated to determine whether an event was a neutron and in what position it interacted in the scintillator. The FPGA card communicates with a PC via a USB.

Figure 1 shows an ISIS WLS fibre test detector with the cover of the electronics compartment removed, together with a close up of the detector back plate. Two 8-channel pre-amp/comparator cards are inserted onto the back of each 16-channel MA PMT. The FPGA card and the low voltage power supply cards are shown in Figure 2. These are mounted on the back plate of the detector box. The design allows the electronics to be interchanged easily from one detector to another for comparison purposes.

Figure 1. LHS: An ISIS WLS fibre test detector showing the PMT assembly and electronics. RHS: A close up of the detector back plate with the electronics.

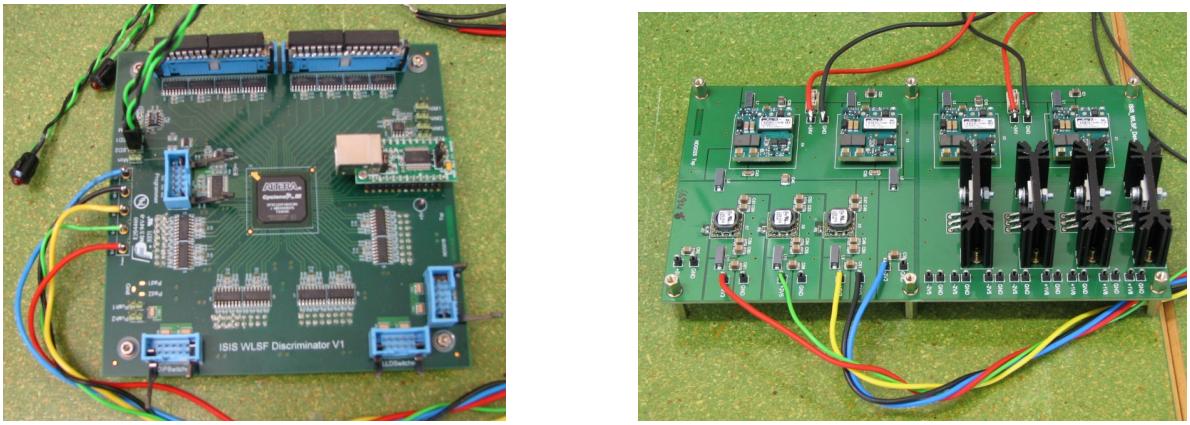

Figure 2. LHS: The original 32 channel ISIS FPGA card which carries out DSP, neutron discrimination and position determination. RHS: The low voltage distribution card.

In the original version of the electronics the FPGA card was completely designed at the component level and can handle 32 PMT signals. A second version has been developed based on a commercial Enclustra FPGA module, complete with USB and Ethernet outputs. The Enclustra module uses a Cyclone 4 EP4CE115 FPGA form Altera. This card, shown in Figure 3, can handle 64 PMT signals. As part of the design upgrade of the electronics hardware, the pre amp comparator cards have been modified with Ethernet outputs, which has improved system reliability and immunity to noise pick-up.

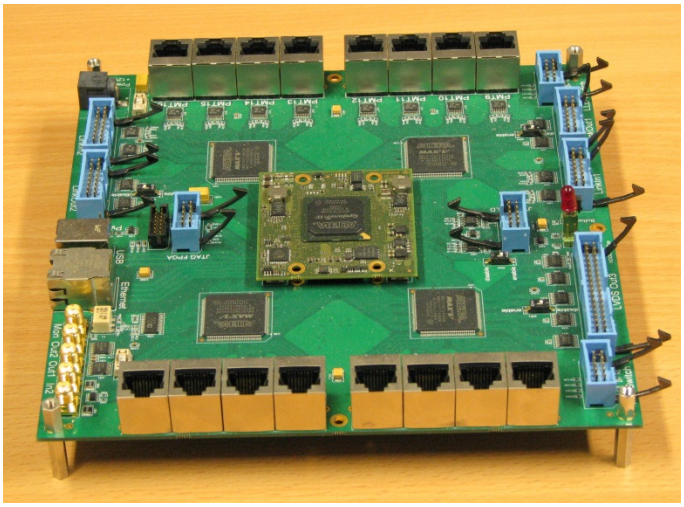

Figure 3. The new 64 channel ISIS FPGA card with the Enclustra daughter board.

The system is working well and allows detector performance to be characterised according to the fibre code, scintillator configuration, PMT type and signal processing algorithm.

The Jülich detector electronics hardware

The Jülich detector electronics is based on three boards, the PMT board, the ASIC board and the FPGA board as shown in Figure 4. The ASIC selected to read out the photomultiplier signals is the Multi-Anode ReadOut Chip (MAROC) which is available from Omega. This chip was designed to readout 64 channels of a multi anode photomultiplier. First, each of the 64 input signals can be amplified by an 8 bit variable gain preamplifier, which has low noise and low input impedance to reduce the crosstalk between the channels. The output current can feed a slow shaper with two sample and hold mechanisms. A digitized 8, 10 or 12 bit output signal is provided by a Wilkinson ADC for any one of the 64 channels. In parallel, all 64 trigger outputs from the MAROC are produced by unipolar or bipolar fast shaping amplifiers, which are connected to adjustable discriminators via a 10 bit DAC. These fast shaping amplifiers are used for the photon counting. Another possible path for photon counting is a fast bipolar shaper with a lower gain, which is also connected to the discriminators to generate the digital output signals.

The MAROC board itself is connected to the FPGA board and the FPGA board is connected via an optical link for data transfer to the DAQ system on a standard computer with a dedicated software environment. The 1,25 GBit optical link was used for the communication with the FPGA and to control and setup the MAROC to optimize the MaPMT readout. After first tests with the electronics, it was decided to change to another standard interface of the FPGA board. Serial ATA (SATA) is a computer bus interface that connects host bus adapters to mass storage devices such as hard disk drives and optical drives and can be easily implemented in our FPGA code connected to the readout interface (SIS1100/PSF1100). The Serial ATA Revision 3.1 specifications increase the maximum data transfer rate from 1,25 gigabits per second (optical link) to 6 Gb/s and adds new features. SATA architecture uses point-to-point connections that allows each device (MaPMT module) to communicate with a host without waiting. SATA uses low voltage differential (LVD) signalling to address the electrical interference and signal integrity issues of parallel ATA. The LVD signalling scheme

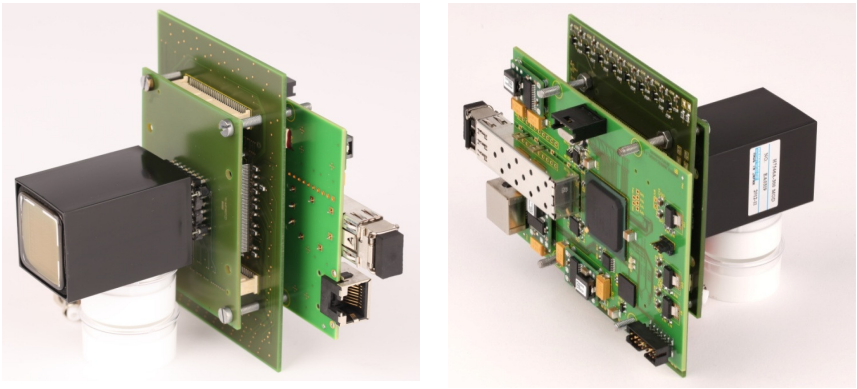

Figure 4: On the left side one can see the boards attached to the MaPMT in the front. The FPGA board with the optical link is shown on the right side.

uses two pairs of data lines to transmit low-voltage signals between the SATA device on the FPGA board and the Concentrator board which reads out several FPGA boards (see Figure 5). The voltage potential between each wire pair represents a data bit. SATA technology allows smaller connectors, cabling, and device form factors to be used, while lowering power consumption.

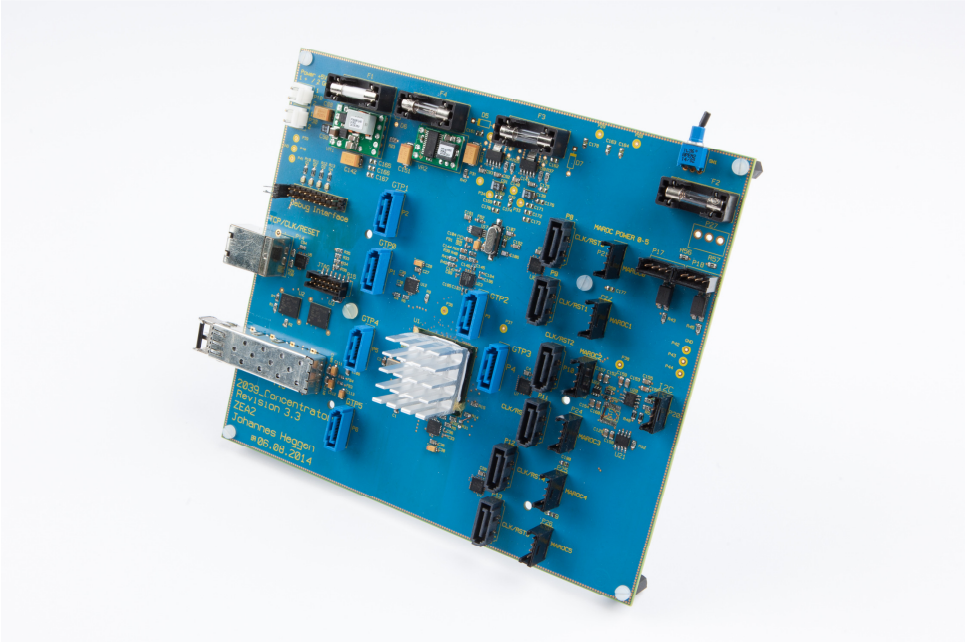

Figure 5: The Concentrator board with SATA connections for the MaPMT modules and an optical fibre link to the PC

The Concentrator board also hosts an FPGA and performs the pre-processing of the data from the FPGA boards of the MaPMTs. In addition, it transfers the data via an optical interface to the DAQ system (PC).

This electronics has been connected to the smaller WLS fibre detector developed at Jülich. This detector has a sensitive area of 5 x 5 cm^2. The 8 x 8 channel pixelated photomultiplier H7546 300 (from Hamamatsu) was coupled to a grid of two orthogonal fibre layers as shown in Figure 6. The final larger detector will use five of these systems to readout the whole detector.

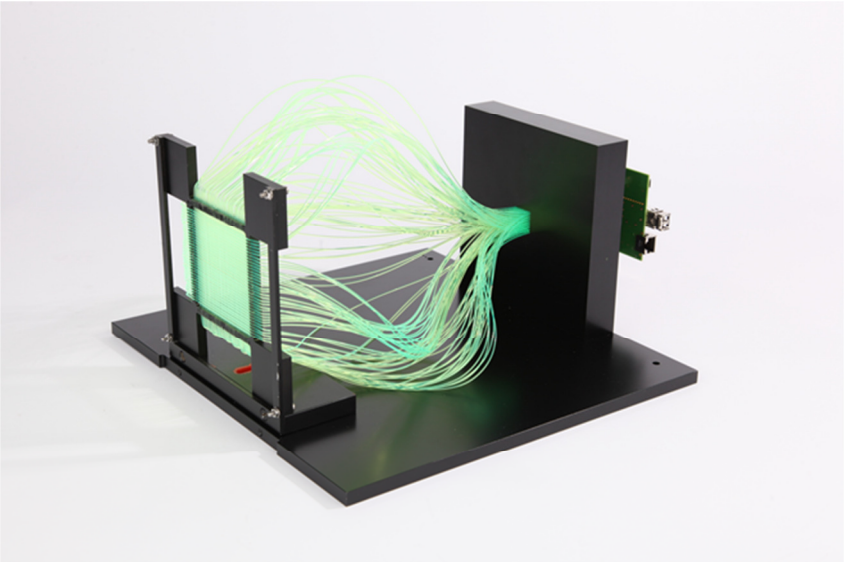

Figure 6: The prototype detector with a 32 fibre grid per layer and double ended fibre readout. The readout electronics is on the right hand side of the picture and the fibre connector to the PC can be seen.

In addition to the designed readout electronics, a Detector Pulse Simulator was developed as shown in Figure 7. The Detector Pulse Simulator has 64 outputs that can be programmed to mimic the signals from the photomultiplier. Different test patterns can be easily selected with the input panel and loaded from an 8Mbyte RAM. This Detector Pulse Simulator has been used to test the electronics chain. By selecting the appropriate test pattern, the electronics chain can be easily calibrated using this simulator. The Detector Pulse Simulator was also needed to optimize the signal processing algorithm for the readout electronics.

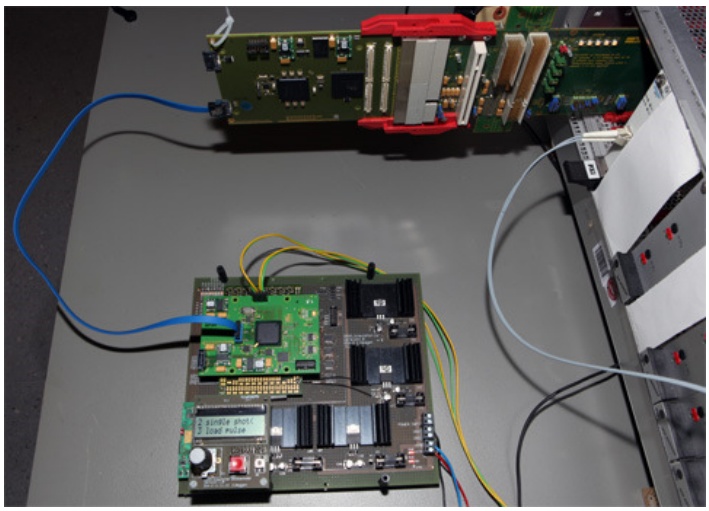

Figure 7: The FPGA readout board hooked on to the 64 channel simulator board and connected via the blue SATA cable to the CPCI read out board.

Conclusions

These two electronics systems provide powerful tools for evaluating detector performance and developing more sophisticated methods of signal processing for both current and future generations of detector. Both systems are suitable for deployment in large numbers, enabling large area scintillation detectors with many channels of photomultipliers to be realised in a cost effective manner.