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The Jülich detector electronics hardware

The Jülich detector electronics is based on three boards, the PMT board, the ASIC board and the FPGA board as shown in Figure 1. The ASIC selected to read out the photomultiplier signals is the Multi-Anode ReadOut Chip (MAROC) which is available from Omega. This chip was designed to readout 64 channels of a multi anode photomultiplier. First, each of the 64 input signals can be amplified by an 8 bit variable gain preamplifier, which has low noise and low input impedance to reduce the crosstalk between the channels. The output current can feed a slow shaper with two sample and hold mechanisms. A digitized 8, 10 or 12 bit output signal is provided by a Wilkinson ADC for any one of the 64 channels. In parallel, all 64 trigger outputs from the MAROC are produced by unipolar or bipolar fast shaping amplifiers, which are connected to adjustable discriminators via a 10 bit DAC. These fast shaping amplifiers are used for the photon counting. Another possible path for photon counting is a fast bipolar shaper with a lower gain, which is also connected to the discriminators to generate the digital output signals.

The MAROC board itself is connected to the FPGA board and the FPGA board is connected via an optical link for data transfer to the DAQ system on a standard computer with a dedicated software environment. The 1,25 GBit optical link was used for communication with the FPGA and to control and setup the MAROC, to optimize the MaPMT readout. After first tests with the electronics, it was decided to change to another standard interface of the FPGA board. Serial ATA (SATA) is a computer bus interface that connects host bus adapters to mass storage devices such as hard disk drives and optical drives and can be easily implemented in our FPGA code connected to the readout interface (SIS1100/PSF1100). The Serial ATA Revision 3.1 specifications increase the maximum data transfer rate from 1,25 gigabits per second (optical link) to 6 Gb/s and adds new features. SATA architecture uses point-to-point connections that allows each device (MaPMT module) to communicate with a host without waiting. SATA uses low voltage differential (LVD) signalling to address the electrical interference and signal integrity issues of parallel ATA. The LVD signalling scheme

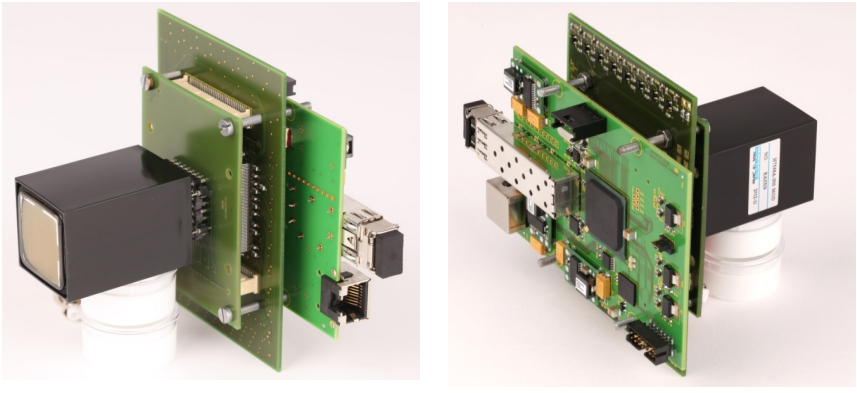

Figure 1: On the left side one can see the boards attached to the MaPMT in the front. The FPGA board with the optical link is shown on the right side.

uses two pairs of data lines to transmit low-voltage signals between the host port and the SATA device. The voltage potential between each wire pair represents a data bit. SATA technology allows smaller connectors, cabling, and device form factors to be used, while lowering power consumption.